TRANSLATION OF KOREAN PRIORITY APPLICATION NO. 10-2003-0022107

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METHOD OF FABRICATING SEMICONDUCTOR DEVICE HAVING SUBMICRON LINEWIDTH

SUMMARY

[Abstract]

The present invention relates to a method of fabricating a semiconductor device using a hard mask and, more particularly, a semiconductor device fabrication method which can form a submicron linewidth using a hard mask and an existing light source. By depositing oxide, polysilicon, and a hard mask on a substrate and performing a patterning process, the present invention embodies a semiconductor device having a submicron linewidth using the hard mask as a mask and an existing light source, thereby realizing expandability of process, extension of generality, and maximization of productivity in a production line.

[Representative Drawing]
Fig. 2

[Index Word]
Hard mask, KrF, ArF, gate electrode, plasma etch

SPECIFICATION

[Title of the invention]
Method of Fabricating Semiconductor Device having Submicron Linewidth

[Brief description of the drawings]

Fig. 1 is a cross-sectional view illustrating a process of depositing and patterning oxide, polysilicon, a hard mask, and photoresist on a semiconductor substrate.

Fig. 2 is a cross-sectional view illustrating a process of performing an isotropic etching for the structure of Fig. 1.

Fig. 3 is a cross-sectional view illustrating a process of removing the photoresist.

Fig. 4 is a cross-sectional view illustrating a process of etching the polysilicon by using a pattern of the hard mask.

Fig. 5 is a cross-sectional view illustrating a process of depositing a nitride layer on the structure of Fig. 4 and forming spacers.

Fig. 6 is a cross-sectional view illustrating a process of removing the hard mask.

[Detailed description of the invention]

[Object of the invention]

[Technical field of the invention and background of the related art]

The present invention relates to a method of fabricating a semiconductor device using a hard mask and, more particularly, to a method of fabricating a semiconductor device having a submicron linewidth by using a hard mask and an existing light source.

Photolithography is a micro processing technology which has supported a progress of semiconductor device industry. Resolution enhancement in the photolithography is in charge of the future of high-integration semiconductor device.

Lithography is generally a patterning process and divided into a photo process and an engraving process. In recent years, however, lithography has come to mean only the photo process, and is classified into optical and non-optical lithography based on a used light source. In a semiconductor device process, the lithography is a technology to form a circuit on a substrate, comprising processes of coating photoresist on a substrate, transmitting light through a mask so that the photoresist reacts with the light, developing the photoresist to form a pattern, and embodying a desired pattern by engraving the substrate with the photoresist pattern.

The degree of integration of a semiconductor chip has increased by a factor of about 4 times every 3 years. In the photolithography process, there have been many developments in materials such as CAR (chemically amplified resist), in processing aspects such as TLR (tri-layer resist), BLR (bi-layer resist), TSI (top-surface imaging), ARC (anti-reflective coating), etc., and in mask aspects such as a PSM (phase shift mask), OPC (optical proximity correction) etc., as well as in exposure equipment itself such as a lens having high numerical aperture and hardware.

Early generation exposure equipment included a contact printer that employed an exposing method, where a mask was located on an upper portion of a substrate to be close to the substrate, and an operator manually adjusted the focus of the optical system with the naked eye. Then, as the technology developed, the resolution was enhanced by reducing the gap between the mask and the substrate, and exposure was achieved through soft contact or hard contact (lower than 10 μm), according to the gap size.

In the early 1970s, a projection-type exposure equipment, which employed an optical system using reflection or refraction, was developed. Accordingly, advancements such as improvement of resolution and an increase in the life of a mask as well as wafer size scale-up, were actively applied to product developments. After that, in the mid-1970s, a stepper applying projection optics was developed to substantially contribute to mass production of semiconductors.

The stepper, adopting an exposure method of "step and repetition," made a turning point in the development of photolithography. By using exposure equipment adopting the stepper method, accuracy in setting as well as resolution was enhanced. The early stepper adopted a reducing projection exposure method using a mask to be patterned on a substrate by a reduction

ratio of about 5:1 or about 10:1. However, the ratio of about 5:1 became gradually in common use due to limitations in mask pattern and size.

In early 1990s, a scanner adopting an exposure method of "step and scanning" was developed. The scanner type exposure equipment was able to cope with increasing chip size and raise productivity, although it put a heavy burden on a mask pattern by using a reduction ratio of 4:1. The resolution of photolithography is closely related to a wavelength of a light source. Early exposure equipment using g-line (λ=436nm) was able to form a pattern of about 0.5 ㎛, and exposure equipment using i-line (λ=365nm) was able to form a pattern of about 0.3 ㎛.

Recently, exposure equipment using a KrF laser (λ=248nm) as a light source, new photoresist materials and development of incidental technologies have made it possible to form a pattern having a design rule lower than 150 nm.

Now, developing technology is capable of forming a fine pattern less than 110 nm by using exposure equipment employing an ArF laser (λ=193nm). DUV (Deep ultra-violet) photolithography has high resolution and a good DOF (depth of focus) property compared to the i-line, but it is difficult to control processes. Such a process control problem may be optically caused by a short wavelength and chemically by using a chemically amplified photoresist. As the wavelength becomes shorter, a CD (critical dimension) tilting phenomenon due to a static wave effect and an engraving phenomenon of reflective light due to a substrate phase become more severe.

In fabricating a semiconductor device having a submicron linewidth, which cannot be formed by existing equipment, a method to solve limitations of a photolithography process is to adjust bias, i.e., difference between a value of critical dimension of the photoresist pattern before etching (DI CD) and a value of critical dimension after etching (FI CD). However, although this method is used, it is not easy to cope with a margin of linewidth that is being reduced.

Accordingly, the present invention solves this problem by using a hard mask and embodies a method of manufacturing semiconductor device having a submicron linewidth which cannot be formed by using an existing light source.

One embodiment is presented to describe the present invention in detail although the present invention can be embodied by various methods.

For example, when a gate having 90 nm linewidth is formed by using existing KrF equipment, a marginal linewidth patterned by a photolithography process is about 125 nm and, therefore, the difference 35 nm has to be removed by an etching process. In view of a DUV photoresist height (PR height), this is an impossible process. Accordingly, a special method, for example, using an ArF scanner, is required. That is, in the KrF process, a height of photoresist has to be less than 3000Å considering a DOF (depth of focus) margin although 125 nm linewidth is patterned.

As a result, to achieve a gate CD (channel length) of 90 nm, the difference 35 nm has to be removed by an etching process. Therefore, each side of a gate pattern has to be cut by 17.5 nm by using photoresist, but in this case a uniform gate device cannot be formed because of an etching speed ratio of gate material to photoresist.

To solve such a problem, a hard mask layer is formed on an etch-target layer and a PR pattern is formed on the hard mask. The PR pattern is formed more thinly than a conventional PR pattern. Next, an etching process is performed using the PR pattern to form a hard mask pattern having the same size as the PR pattern.

Then, the etch-target layer is etched using the hard mask pattern as a mask to form an etch-target layer pattern having a desired size.

A hard mask process is widely used in an existing DRAM manufacturing process, but in case of logic products employing a salicide (self-aligned silicide) process, a hard mask cannot be used to perform because salicide has to be formed on a gate.

[Technical problem]

Accordingly, the present invention is directed to a method of fabricating a semiconductor device having a submicron linewidth that substantially obviates one or more problems due to limitations and disadvantages of the related art. An object of the present invention is to embody a submicron linewidth, which cannot be formed by an existing light source, by applying a hard mask process to logic products.

[Disclosure of the invention]

The object of the present invention is achieved by a method of fabricating a semiconductor device having a submicron linewidth, comprising depositing oxide (11), polysilicon (12), a hard mask (13), and photoresist (15) on a substrate (10), patterning the hard mask (13), and etching the polysilicon (12) using a pattern formed through the hard mask (13).

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Figs. 1 through 6 illustrate a semiconductor device fabrication process in accordance with the present invention.

Fig. 1 is a cross-sectional view illustrating a patterning process using a photoresist mask.

.First, oxide (11), polysilicon (12), a hard mask (13) and photoresist (15) are deposited on a semiconductor substrate (10). The photoresist (15) is patterned by using a mask to form a structure of Fig. 1.

The photoresist (15) is patterned by using a KrF light source so that a resulting photoresist pattern has a width of 120 nm (A).

The hard mask (13) is formed of PE-oxide.

An anti-reflection coating (ARC) (14) to reduce reflexibility may be further deposited on the hard mask. The anti-reflection coating is formed of organic or inorganic ARC.

Fig. 2 is a cross-sectional view illustrating a process of etching the hard mask using a plasma etching.

The anti-reflection coating (14) and the hard mask (13) are etched by using plasma and the photoresist pattern (15) as an etching mask.

The plasma etching is an isotropic etch using SF_6 gas, and etches in sequence the anti-reflection coating (14) and hard mask (13).

Fig. 3 is a cross-sectional view illustrating a process of removing the photoresist and anti-reflection coating through ashing/strip processes.

After the plasma etching, the photoresist and anti-reflection coating are removed by ashing/strip processes.

Fig. 4 is a cross-sectional view illustrating a process of etching the ploysilicon by plasma etching to make a gate electrode.

To form a gate electrode, the polysilicon (12) is etched by a plasma etching using a hard mask pattern obtained after the ashing/strip processes, as an etching mask.

The plasma etching uses Cl_2/HBr, Cl_2/O_2, or HBr/O_2 as an etching gas. Here, an etching speed ratio of polysilicon:oxide is preferably 10:1. A gate electrode formed has a width of 80 nm.

Fig. 5 is a cross-sectional view illustrating a process of forming of spacers (17). An oxide layer (16) and nitride layer are in sequence deposited on the substrate having the gate electrode. The nitride layer is etched by an etch back process to form spacers (17).

The nitride layer is SiN.

Fig. 6 is a cross-sectional view illustrating a process of removing the hard mask (13).

After formation of the spacers (17), the hard mask (13) and the oxide layer (16) are removed by a wet etching.

In manufacturing a gate electrode of logic product, the above-described process can form a gate electrode having a linewidth of 90 nm by using an existing KrF light source and a hard mask instead of a photoresist mask.

The foregoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to

limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.

[Effect of Invention]

Accordingly, by using a hard mask instead of a photoresist mask and existing equipment without additional investments and controlling a required linewidth by products through an etching process in forming a gate electrode, a semiconductor device fabrication method according to the present invention embodies a product having a submicron linewidth. Thus, the present invention can realize expandability of process, extension of generality, and maximization of productivity in the production line.

CLAIMS

【Claim 1】

A method of fabricating a semiconductor device comprising:

a first step of forming oxide (11) on a substrate (10);

a second step of forming polysilicon (12) on the oxide (11);

a third step of forming a hard mask (13) on the polysilicon (12);

a fourth step of depositing photoresist (15) on the hard mask (13) and patterning the photoresist; and

a fifth step of etching the polisilicon (12) using a pattern formed through the hard mask (13).

【Claim 2】

The method as defined by claim 1, further comprising a step of depositing an anti-reflection coating on the hard mask to reduce reflexibility.

【Claim 3】

The method as defined by claim 2, wherein the anti-reflection coating is formed of an organic or inorganic ARC.

【Claim 4】

The method as defined by claim 1, wherein patterning the photoresist in the fourth step is performed by using a KrF light source.

【Claim 5】

The method as defined by claim 1, wherein the hard mask is formed of PE-oxide.

【Claim 6】

The method as defined by claim 1, wherein the pattern formed through the hard mask (13) in the fifth step is formed by etching the hard mask using a patterned photoresist as an etching mask.

【Claim 7】

The method as defined by claim 6, wherein etching the hard mask is an isotropic etching.

【Claim 8】

The method as defined by claim 7, wherein the isotropic etching is a plasma etching.

【Claim 9】

The method as defined by claim 8, wherein the plasma etching uses SF_6 gas.

【Claim 10】

The method as defined by claim 1, wherein etching the polysilicon in the fifth step uses a plasma etching.

【Claim 11】

The method as defined by claim 10, wherein the plasma etching uses Cl_2/HBr, Cl_2/O_2 or HBr/O_2 as an etching gas so that an etching speed ratio of polysilicon : oxide is 10:1.

【Claim 12】

A semiconductor device comprising a gate electrode formed by the method of claim 1.

DRAWINGS

Fig. 1

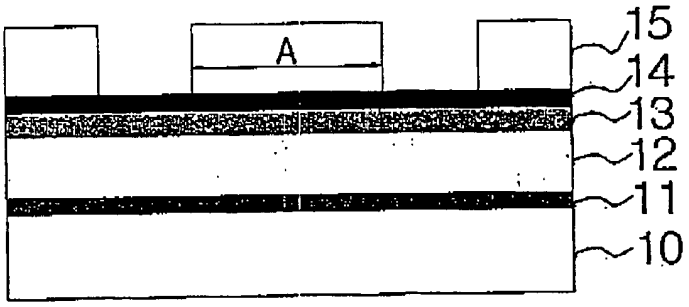


Fig. 2

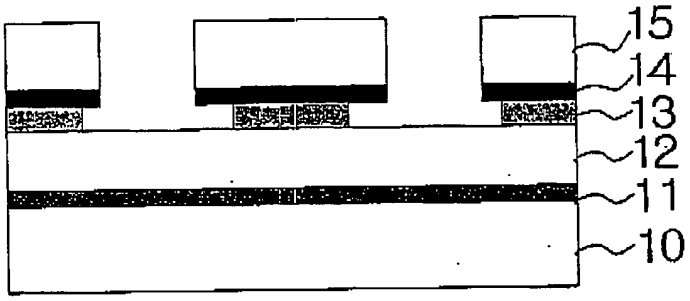


Fig. 3

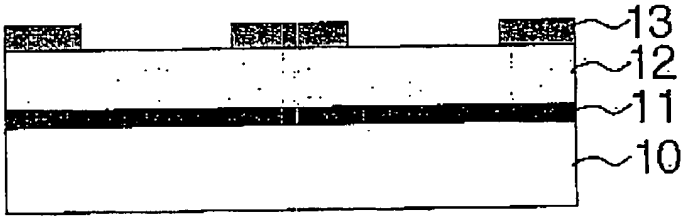


Fig. 4

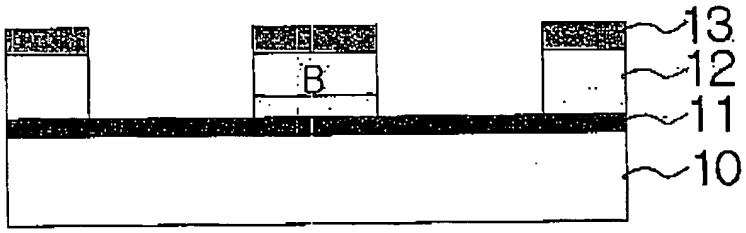


Fig. 5

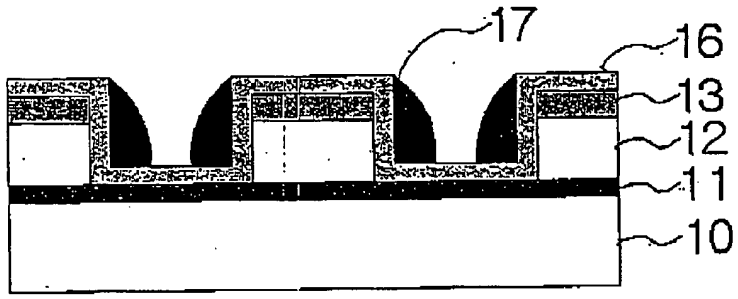
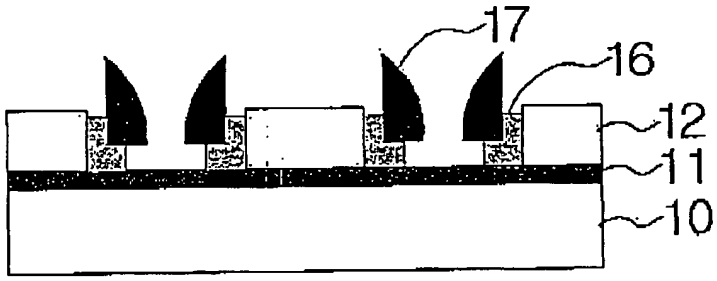


Fig. 6



I, So-Young OH, hereby certify that I am familiar with the Korean and English languages, and that the attached is a true and accurate translation of Korean Application 10-2003-0022107.

Date: September 15, 2005 Signature _____

Name So-Young OH